



MORPHEUS

Abstract of D5.4: Evaluation Report of phase 1

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ABSTRACT	This document is the abstract of the D5.4 It is available on the MORPHEUS public website
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In this document the experiences are collected which have been gained during the phase 1 of the MORPHEUS project. Three applications, which are to be ported to the MORPHEUS platform in phase 2, have been implemented on COTS.

The first system by Alcatel-Lucent relies on two Xilinx development boards. Realization of the targeted application as described in more detail in section 3.1 turned out to be more complicated than anticipated. Nevertheless the concept was proved and thus a migration of this application to the MORPHEUS platform seems feasible. Numerous design details ran into other work packages, namely WP3/WP4, which defines the architecture of the MORPHEUS chip.

The phase 1 development of the second system by DTO, the implementation of a noise grain removal algorithm, is based on an FPGA board as well. They experienced the same, typical effect, that development took longer than anticipated. Thus, with the availability of a chip like the MORPHEUS platform, both application partners implicitly count on a development cycle reduction.

The phase 1 development of the TOSA application, the implementation of a motion detection algorithm, is based on a SIMD parallel processing platform itself implemented on a FPGA board. Good productivity results were obtained on the top of this platform but the development of the platform itself required a large amount of efforts.

In the following chapters the work which has been done is described in detail. Each section ends with a description of the experience gained during the application development phase and a recommendation list. Finally the concluding section summarizes the results of phase 1.

