



# MORPHEUS

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## **Abstract of D3.5: Description of the reference simulation environment**

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ABSTRACT	This document is the abstract of the D3.5 It is available on the MORPHEUS public website
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This deliverable presents the MORPHEUS HDL reference simulation environment that is used as final simulator reference for early application development. Its Verilog gate-level equivalent extracted from the chip layout (with relative parasitic delay) is used for hardware verification. The HDL simulator is complete which means that all components of the MORPHEUS chip are integrated into this simulator.

The MORPHEUS reference simulator is the basis of the MORPHEUS simulation concept since it ensures fully conformance with the MORPHEUS chip implementation.

In this deliverable, the organization and guidelines for the installation of the HDL reference simulator are presented. The usage of the simulator and its main functions is shown on the basis of a reference example.

