



MORPHEUS

Abstract of D4.2: MORPHEUS roadmap refinement report completed by modularity objectives

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ABSTRACT	This document is the abstract of the D4.2. It is available on the MORPHEUS public website
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This document describes the refinement induced by the Roadmap monitoring refinement activity relative to task 4.1 of WP4 over the Architecture design and implementation in MORPHEUS.

According to the orientation described in the MORPHEUS "Roadmap Monitoring Report" [1], that is the main reference for this roadmap refinement,

"The MORPHEUS platform is a complex System-on-Chip that exploits run-time programmability at different levels to provide a competitive computing solution, which can challenge developments costs of application specific silicon platforms through product customisation after fabrication. MORPHEUS ambition is to deliver computational power competitive with state-of-the-art programmable Systems-on-Chip maintaining flexibility to a broad spectrum of applications, and user-friendliness."

As such, MORPHEUS should be compared to state-of-art signal processor engines, as again suggested in [1]

a) *Commercial FPGA-based processing platforms such as Xilinx Virtex and Altera Stratix.*

b) *DSP oriented programmable systems-on-chip such as OMAP by TI, Nomadik (STn88xx) by ST, PXA and Cell by IBM/Sony/Toshiba.*

c) *Interconnect-oriented multicore platforms, such as RAW by MIT, Imagine by Stanford University, PicoChip, Pleiades by UCB.*

The metrics for evaluating the chip design and the relative roadmap must be defined according to the above introduction, and can be summarized as follow in a strictly hierarchical order:

1) **Computational power in order to sustain real-time constraints imposed by the chosen reference applications.** MOPS/MHZ, MOPS/mW, processed Bits/Sec and Processed Bits/Joule can be a reference not as absolute values but only as related to the set of reference applications and the relative real-time and market constraints.

2) **User programming proficiency in order to allow the ordinary user to exploit effectively, and with good productivity, the available computational power.** The "time to market" for a given application can not possibly be that of a software programmable machine, but it must be comparable to software costs and not to standard hardware – oriented development as it is the case for FPGAs.

3) **Silicon Implementability.** MORPHEUS is not a purely research oriented task. A silicon prototype is being realized and relevant industrial partner look at MORPHEUS as a possible "pipecleaning" activity. For this reason, many architectural choices have been steered (or "refined") in order to take into account factors as economic convenience, integration costs (NRE costs and silicon real estate), time to market of the proposed hardware platform and so.

In addition to the design orientation expressed above, further refinements were suggested in the course of the first 18/24 months of the project by application development and by the practical implementation of the initial guidelines. To these factors, some specific occurrence such as evolution of foundry calendars, deadline readjustments, unplanned manpower overloads have also suggested roadmap refinements. The present document will describe all roadmap refinements implemented on the MORPHEUS chip architecture and concept in the course of the first 24 months of the project, as well as a revision of the modularity objectives as planned for the remainder of the project lifetime. In the following,

- chapter 2 will provide a description of the refinement of the architectural concept as a whole due to feedback from state-of-art, work-package interaction and roadmap monitoring, focusing mostly on architecture and design issues

- chapter 3 will provide an insight on the specific roadmap refinement relative to the most significant IP blocks that are being developed/integrate in the design.

- chapter 4 will provide a description of the refinement that were necessary to the project calendar, and propose also a revision of the timelines and modularity objectives for the remainder of the project.

The roadmap revision with respect to the evaluations described in [8] is completed by deliverable D2.1.2 [2]. While this document focuses essentially on the MORPHEUS concept, architecture and user programming model, D2.1.2 is oriented to the "revised toolset specification".

