



# MORPHEUS

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## Abstract of D6.7: Exploitation Plan

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ABSTRACT	This document is the abstract of the D6.7. It is available on the MORPHEUS public website
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This document presents an overview about the exploitation within the MORPHEUS project after the second year since the beginning of the project.

The introduction (section 2) presents the definition of exploitation and answers to the exploitation issues: who will exploit and disseminate what knowledge, how, when, why and to whom?

Exploitation is made by all the project partners: large industries, SMEs and research centres or universities. The perspective of exploitation of every participant is summarized in a table.

Exploitation plans resulted more effective involving marketing experts; the best effect is obtained by a joint effort of marketing and technical people.

Section 3 deals with the issue of Intellectual Property Rights (IPR). After summarizing the principles ruling the IPR issue from the contract, it analyzes the current situation within the project. All the IPR issues are solved and the necessary access rights are granted for the project time frame and the purpose of building the MORPHEUS SoC that is just a demonstrator. All other issues exceeding the project's purpose (as building a commercial product) or its time frame will be dealt with by following agreements that will take as a basis the MORPHEUS contract.

The report develops, in section 4, the exploitation plan of every single partner. The project partners have different exploitation possibilities depending on their main field of activity.

- Large industrial partners are mainly interested in internal exploitation; they foster innovation through contacts with their business units. Some large companies are aimed at obtaining proof-of-concept out of the MORPHEUS project for further developments.

- SMEs are contacting new customers, increasing the size of the company, developing new partnerships, sustaining their product roadmap, sustaining new projects and are aimed to obtain increased visibility.

- Universities are using the results of the project improving curricula of regular courses and to set up exercise/laboratory sessions, improving the quality of engineering education. They are also giving rise to new projects and exploiting knowledge through patents.

ST presents its internal exploitation of the PiCoGA-DREAM platform and of the SpiderGON NoC.

ST's exploitation strategy involves the collaboration of internal business units such as the wireline division or groups that are performing evaluating the platform with applications. Another important outcome of the MORPHEUS partnership is the experimentation of the PiCoGA module for THALES telecommunication applications.

PACT presents the roadmap of its XPP-III architecture, the business model and plan are showing growing revenues from the XPP architecture rising from 2M€ in 2007 to 9 M€ in 2008 and 30 M€ in 2009. They present a market analysis by target markets. They describe customers' needs that want to replace ASIC design with flexible programmable units. PACT has also a university program to promote its platform. PACT participates to MORPHEUS to increase visibility. The MORPHEUS project will increase the acceptance of reconfigurable computing solutions: a silicon implementation is mandatory for customer acceptance.

M2000 presents the exploitation about its eFPGA. Its inclusion in the MORPHEUS chip is a strong reference for M2000. Today's business model is to supply embedded FPGAs hard macros. It will be complemented by the direct sales of the new family of FPGA devices. The company is interested in attracting the Venture Capital firms. M2000 has grown from 19 people in Q3 2006 to 48 at the end of 2007 and plans to reach more than 60 people in 2008. The target markets are presented for eFPGA and FPGA. M2000 lists various benefits from the participation to MORPHEUS such as: availability of a complete demonstrator platform (including hardware, software and applications), increased visibility on the market and improved industrial relations.

CBLUE wants to work closely with academic and industrial partners to enhance its tools. CBLUE has a commercial interest in reconfigurable architectures as this area will be a significant long term market opportunity. CBLUE believes that the availability of efficient tools for mapping software applications onto reconfigurable fabrics is a vital element that will ultimately produce significant endproduct and designer benefits. The technologies being developed within the consortium are highly complementary to CBLUE's existing tools. The MORPHEUS project allows CBLUE to develop a high level of interoperability with these other tools and to make significant improvements to its Cascade tool to improve its targeting of reconfigurable architectures. CBLUE believes that this will widen the appeal of its own offering and will validate and grow the overall market opportunity for European reconfigurable fabric and tools vendors.



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ACE in the MORPHEUS project wants to expand its knowledge and expertise in the field of compilation for reconfigurable processor architectures and parallel processor architectures. ACE wants to extend its existing CoSy compiler development system product with generic support for reconfigurable architectures and parallel architectures.

TRT develops links with THALES business units for the exploitation of the MORPHEUS results. The role of TRT is to provide competitive advantages to THALES through research studies. TRT organizes Techno Days to disseminate new technologies to THALES business units. The exploitation perspectives of the MORPHEUS project are mainly for proposing advanced reconfiguration concepts. The MORPHEUS platform will offer a state-of-the-art sustainable reconfigurable solution for THALES's computing applications.

DTO researches technologies acts as strategic market consultant for Thomson BUs beyond 2 years time frame. DTO choose the film grain removal application, from Grass Valley Production and Postproduction Solutions to demonstrate the benefits of the MORPHEUS approach. The GV PPS market is characterized by very high end applications, low volumes, high prices, high data rates and sophisticated solutions. GV PPS offers equipment of complete range of high-quality solutions for acquisition, conversion, post production, and delivery systems for multiple formats. Typical customers are film post production firms. Higher scanning speed and resolution, better image stability, faster image processing solutions, automated workflows are main challenges for future products. MORPHEUS can enable the development of very flexible image processing architectures which can be reprogrammed for many different applications. Using such technologies would enable GV PPS to address many different product niches with the same platform, which was only possible from software solutions.

ICOM analyzes the market drivers leading to a wireless instead of a wired solution. The application targeted by INTRACOM S.A. Telecom Solutions is the emerging IEEE 802.16j broadband mobile wireless standard. ICOM has a wide portfolio of solutions including wireless access network infrastructure and is poised to promote the use of broadband wireless access, in full co-operation to wire-line broadband access networks. At present, the company's products are sold in over 50 countries, including the Eastern Europe region, the Americas and the Middle East. For many products, reconfiguration is a key factor for commercial success. The IEEE 802.16j broadband mobile wireless system is a demanding application which requires dynamic reconfiguration. Therefore, ICOM will prove the capabilities of MORPHEUS on application that is beyond the stateof the-art. The main goal of ICOM is to use the IEEE 802.16j system as a proof of concept for applying MORPHEUS reconfiguration concepts. In parallel, ICOM envisages to apply these concepts in other wireless products of the same family as well.

ALCATEL-LUCENT presents its exploitation perspectives for reconfigurable systems-on-chip in telecommunication networks. The market trends indicate that there will be an evolution towards the "All-IP" network of the future where services drive technical innovation. Reconfigurable SoC can provide fundamental contribution to meet the user expectations facing the technical challenges. Reconfigurable computing will correspond to early market presence and shorten development cycle developing products before standards are stable. In the MORPHEUS project the contribution of ALCATEL-LUCENT mainly consists of the development of a concept for updating the hardware of installed network elements partially, a patent for this concept is currently pending. In phase 1 of the project, a demonstrator based on two FPGA evaluation boards is built in order to proof the concept. In phase 2 the application is ported to the MORPHEUS platform. ALCATEL-LUCENT is not intending to use MORPHEUS chip as a product but only a demonstrator to prove a concept, moreover since the MORPHEUS chip will not be a commercial product, it will have to be adapted to the needs of the applications later on. ALCATEL-LUCENT does not expect to need all the parts of MORPHEUS chip, PACT component for example will not be necessary for them. MORPHEUS chip could then be scaled down to be adapted to the needs. The ALCATEL-LUCENT application is used to specify capabilities requirements for the MORPHEUS platform (power requirements, performances, flexibility, etc...).

TOSA intends to perform exploitation for handheld cameras, the MORPHEUS architecture appears to be a better candidate than FPGA since it brings low power consumption in addition to high processing power and strong reconfiguration capabilities. Hence, provided the MORPHEUS architecture confirms these expected benefits, TOSA plans to use such architecture for the handheld camera market.



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UK will exploit the result of the project in particular about the on chip memory architecture, the SoC interconnect infrastructure (using and customizing the NoC) and the dynamic reconfiguration methodologies. The main exploitation activity performed by UK is in the training. The results of MORPHEUS project are used in a set of courses and a system-on-chip laboratory was started since summer 2006 dealing with reconfigurable computing issues. It is planned for practical introduction of the MORPHEUS platform when available. Remaining exploitation issues are related to the exploitation by other projects such as the started "Initiative reconfigurable supercomputing in KIT" and the possibility to reuse the MORPHEUS simulator platform in ÆTHER.

TUD in collaboration with ACE is mainly involved in the retargetable compilation tools for the target platform. One main exploitation result is the implementation in the CoSy compiler of the MOLEN programming paradigm which provides generic support for reconfigurable architectures. An additional exploitation result is the development of research contacts and collaborations with prominent researches in the reconfigurable computing domain in Europe.

CEA-LIST aims at the valorization of research projects results. Valorization is obtained through Publications, Patents, Prototypes, and Products. Reconfigurable architectures are considered as one key technology for embedded computing as they allow a good compromise between flexibility, processing power and consumption. MORPHEUS is the opportunity to extend research activity on reconfigurable architecture towards system management of computing resources. The MORPHEUS project will allow making very important progress in the area of reconfigurable computing. After the end of the project, the results will be used as starting point for more downstream projects and/or industrial collaboration contracts. They will also be integrated within CEA-LIST's internal embedded multi-processor computing platform as an asset for further research actions.

UBO is developing Master courses on software for embedded systems. Some of the developments achieved during MORPHEUS at UBO can be reused inside this course. It is the case for SoC highlevel simulator that allows students to understand relationship between communication delays and bandwidth and computation circuit capabilities, as well as circulation of control information. It is also the case for synthesis and synthesis framework as yet shown from CDFG to M2000 technologies.

UBO contributes to partner efforts to spread reconfigurable technologies in education (initiatives from UK is an example). A one time publication of the software will be done at the end of the project, with the current lab resources, we cannot maintain a free software release. ARCES in collaboration with ST is mainly involved in the definition of the memory infrastructure and in the design of the overall interconnect. The achievements of the MORPHEUS project are used in three different university courses: "Digital Circuit Design", "Architecture for signal processing elaboration" and "Digital Electronics".

TUBS collaborates closely with DTO within the MORPHEUS project. The MORPHEUS project and its results are used in several lectures. The dissemination of the project results is an important task for the institute to raise interest in the MORPHEUS project and to promote the institute itself. The last important factor of the TUBS exploitation plan is the usage of project results for future research projects.

TUC will use MORPHEUS to extend its position in electrical engineering research in Saxony. MORPHEUS will help TUC to understand the reconfiguration algorithms provided by the FPGA vendors enabling TUC to extend and improve these tools.

