



MORPHEUS

Abstract of D3.3: Final specification of the SOC to be implemented in WP4

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ABSTRACT	This document is the abstract of the D3.3 It is available on the MORPHEUS public website
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This document presents the reference description of the MORPHEUS architecture as it is needed by work package 2 (tools) and work package 5 (application mapping). All detail information that is available regarding the MORPHEUS architecture is collected in this document. If new information regarding the architecture comes up or slight architectural modifications will become necessary (e.g. by feedback from back end implementation) this document will be updated. The MORPHEUS hardware architecture is centred on three heterogeneous reconfigurable engines (HREs) targeting different types of computation:

The PACT XPP is a coarse grain reconfigurable array primarily targeting algorithms with huge computational demands but mostly deterministic control- and dataflow. Further enhancements based on multiple, instruction set programmable, VLIW controlled cores featuring multiple asynchronously clustered ALUs also allow efficient inherently sequential bitstream-processing.

The DREAM is based on the PiCoGA core [13][14][15][16]. The PiCoGA is a mediumgrained reconfigurable array consisting of 4-bit oriented ALUs and 4-bit LUTs. The architecture is mostly targeting instruction level parallelism, which can be automatically extracted from a C-subset language called Griffy-C.

The M2000 is a lookup table based fine grain reconfigurable device – also known as embedded Field Programmable Gate Array (eFPGA). As any FPGA, it is capable to map arbitrary logic up to a certain complexity provided register and memory resources are matching the specifics of the implemented logic.

All control, synchronization and housekeeping is handled by an ARM 926EJS embedded RISC processor. As dynamic reconfiguration might impose a significant performance demand for the ARM processor, a dedicated reconfiguration control unit is foreseen to serve as a respective offload-engine. All system modules are interconnected via multilayer AMBA busses. Separate busses are foreseen for reconfiguration and/or control and data access. As the required bandwidth for high performance data intensive processing might become huge, a network on chip (NoC) based on ST's spidergon technology [12] has been integrated.

As the HREs operate on differing clock domains, they are decoupled from the system and interconnect clock domain by data exchange buffers (DEB) consisting of dual ported (dual clocked) memories either configured as FIFOs or pingpong buffers. The HREs have access to further onchip SRAMs for buffering of local data. These SRAMs may be either used as cache or scratchpad RAM. A state of the art multichannel SRAM/Flash controller provides access to external SRAM and Flash memory. To satisfy the huge application requirements regarding memory throughput an advanced DDRAM controller provides access to external DDRAM.

In difference to other approaches the MORPHEUS platform architecture addresses high performance reconfigurable computing for general purpose applications. The heterogeneous HREs support the different flavours of reconfigurable computing which are known as coarse, mid, and fine grain reconfigurable computing. To support a good utilization of all the three reconfigurable engines –even for general purpose– they are interconnected by a high speed NoC, which allows a close coupling of the HREs.

A specialization of the MORPHEUS architecture can be done mainly by dimensioning of the architectural components. Examples for such dimensioning decisions are the adaptation of internal memories or adaptation of the sizes of the reconfigurable processing units to allow more efficient implementation for special application domains. The basic MORPHEUS architecture itself will remain the same.



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