



# MORPHEUS

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## Abstract of D4.5.1: Preliminary description of HDL database

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ABSTRACT	This document is the abstract of the D4.5.1. It is available on the MORPHEUS public website
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The present document describes the structure of the MORPHEUS RTL database at the end of M18, after final functionality specification, but prior to P&R feedback, memory sizes and HRE size finetuning, and final bug fixing after verification.

It represents a reference description of the MORPHEUS Chip architecture, and its design hierarchy. Deliverable 4.4, issued concurrently, will provide an analysis of the chip performance at this stage in terms of expected area, timing and power consumption.

The database, as well as the Chip architecture is organized in a 3-layers hierarchy.

1. The top level corresponds to the System level design, including the connection between main blocks and specification of IOs. The main component blocks of the MORPHEUS testchip can be classified in two categories:

a) Computational Engines

b) Hardware services

*Category (a)* is composed by the 3 **HREs (Heterogeneous Reconfigurable Engines)** that provide to the MORPHEUS platform the computational power, and their connection to the main system:

Pact XPP

M2000 FlexEOS

PiCoGA

Each of these blocks resides in a specific Clock Island with a specific PLL and a safe crossdomain communication mechanism. The clock frequency can be regulated at run-time in order to allow each HRE to perform, according to the required functionality, at the ideal speed.

*Category (b)* comprises the set of **Hardware Services** that are added to the MORPHEUS chip in order to facilitate and enhance the utilization of HREs by the end user

System Control, Debug/Test, Generic IO and Synchronization

Memory hierarchy and System level Data Communication

Configuration Management

High Speed Data Transfer

All these "services" are part of the "main" clock island, whose frequency is regulated by the main PLL at boot time. Both HREs and hardware services are controlled by the user through the main processor (an ARM926EJS core).

2. The second layer is the top level of each single building block, both for what concerns category (a) and (b). In this level data and configuration exchanges between HREs, communication means and the main processor core are handled, as well as HW/SW protocols for the overall system synchronization. The description of this layer will be particularly accurate: we believe that a detailed overall description of synchronization issues from all contributors is a fundamental prerequisite in order to:

a) ensure a smooth chip level integration,

b) Guarantee a safe and homogeneous programming model to the chip end users

3. The third level comprises the specific implementation details for each HRE and hardware service. This layer is voluntarily kept hidden to the main user that should understand the main overall system functionality without having to deal with specific implementation details.

For this reason in most cases this layer will be described only marginally, the only aim of this description being the support for silicon integration issues and verification at chip level (Verification at IP level being responsibility of each contributor).



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