



# MORPHEUS

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## D4.6 Silicon platform and verification report

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ABSTRACT	This document is the abstract of the D4.6. It is available on the MORPHEUS public website
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## Context

This deliverable is part of the MORPHEUS project which is a european initiative financed under the 6th FP and addresses innovative solutions for embedded computing based on dynamically reconfigurable platform and tools.

MORPHEUS project aims at satisfying embedded systems new demanding requirements in terms of computing performance, cost-efficient development, functional flexibility and sustainability by developing a global solution based on a modular heterogeneous SOC platform providing dynamically reconfigurable computing completed by a software oriented design flow and a consistent toolset.

MORPHEUS is a 3-year project started in 2006 and gathering all the required expertises from several countries: academics, industrials, SMEs.

## Aim of the deliverable

This deliverable describes the results of the functional test activity performed on the MORPHEUS silicon samples. The aim of this document is also to be used as reference for the partners involved in application mapping on the test chip.

## Content of the deliverable

The document is divided in two parts. The first one provides a detailed description of the test vector used for the functional verifications on the MORPHEUS chip and a report of each performed test. The second part describes the power measurements performed on the various parts of the chip.

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The chip functional verification was based on a succession of sequential steps, each being prerequisite for the following, and this report follows the same scheme: the deliverable first describes the test vectors used to perform the verification of the ARM processor, together with its tightly coupled memories and the main memory. Then the verification of the peripherals connected with the AMBA BUS such as the two UART ports, GPIOs, and the multi port memory controller. The deliverable then describes the verification of the configuration infrastructure (bus and configuration memories) and to the debug bus (a secondary BUS orthogonal to the NoC infrastructure which accesses all DEBs). Finally the functional verification of the communication infrastructure is reported, consisting of a program that runs different simultaneous transfers from various nodes of the NoC.

The power measurement part of the deliverable describes the test vectors used to perform measurements on each block composing the chip. Each Clock island has been activated and measured separately in order to create a power model for the whole chip assuming the 4 clocks running at different independent frequency. Power measurement was performed using test vectors appositely created to stress the various part of the chip. Hence, the power consumption reported with these test has to be considered as a peak condition, not typically reached by normal applications. The maximum consumption measured by means of these applications is: 0,8 mW/MHz on eFPGA, 2.1mW/MHz on DREAM, 7.6 mW/MHz on XPP, 2.4 mW/MHz for the system considering 1V supply voltage.