



# MORPHEUS

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## Morpheus Project Description D6.4.2

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AUTHOR, COMPANY	Philippe BONNOT (TRT)
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## 1. Introduction

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The purpose of this document is to present a summary of the key elements of the project:

- The objectives
- The IST context
- The technical content according to the final version of the Description of Work
- Projects details
- The participants

## 2. Executive summary

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MORPHEUS stands for Multi-purpOse dynamically Reconfigurable Platform for intensive HEterogeneoUS processing. This project addresses a technology breakthrough for embedded computing by developing a reconfigurable platform and tools.

## 3. Detailed presentation

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### 3.1. FP6 context

Project acronym: **MORPHEUS**

Funded under FP6 (Sixth Framework Programme)

Action Line: IST-2002-2.4.1: Nanoelectronics

### 3.2. Coordination

#### Contact Person:

BONNOT Philippe (replacing EDELIN Gilbert)

Tel: +33-1-69 41 60 59

Fax: +33-1-69 41 60 01

Email: [philippe.bonnot@thalesgroup.com](mailto:philippe.bonnot@thalesgroup.com)

#### Organisation:

THALES Research & Technology France

Route Départementale 128

91767 PALAISEAU Cedex

FRANCE

### 3.3. Content summary

The Multi-purpOse dynamically Reconfigurable Platform for intensive HEterogeneoUS processing (MORPHEUS project) is an integrated project which addresses innovative solutions for embedded computing based on dynamically reconfigurable platform and tools. The large-scale deployment of embedded systems is indeed raising new demanding requirements in terms of computing performance, cost-efficient development, functional flexibility and sustainability. This leads to an increasing complexity of the platforms and an enlarging design productivity gap: current solutions are out of breath while current development and programming tools do not support the time-to-market needs.

MORPHEUS copes with these challenges by developing a global solution based on a modular heterogeneous SOC platform providing the disruptive technology of dynamically reconfigurable computing completed by a software (SW) oriented design flow and a consistent toolset. These "Soft Hardware (HW)" architectures will enable huge computing density improvements (GOPS / mm<sup>2</sup>), reuse capabilities, flexibility and time to market thanks to a convenient programming toolset.

MORPHEUS ambitions to establish the European foundation for a new concept of flexible "domain focused platforms" (the platform architecture is modular and every concrete instantiation can be a specialisation for a certain domain), positioned between general purpose flexible HW and general purpose processors and providing breakthroughs in performance and cost-effectiveness to embedded computing systems. This will be achieved within a 42-month integrated project providing:

- A modular silicon demonstrator composed of complementary run-time reconfigurable building blocks to address the different types of application requirements
- The corresponding integrated design flow supporting the fast exploration of HW and SW alternatives

The suitability and the efficiency will be validated by a set of four complementary test cases: Broadband wireless access, Network routing, Professional video, Homeland security.

The dissemination through silicon offer and supporting tools (baseline for further commercial products) will be completed by specific training and broad information to address the necessary cultural change. This will be performed by a consortium where many partners are already involved in bilateral cooperation, and implemented along a 2-step process to monitor the final content of the project according to state of the art evolution and first results.

### **3.4. Project Details**

Project Acronym: MORPHEUS

Project Reference: 027342

Start Date: 2006-01-01

Duration: 42 months

Project Cost: 15.729 M€

Contract Type: Integrated Project

End date: 2009-06-30

Project status: Execution

Project Funding: 8.240 M€

Website address: <http://www.morpheus-ist.org>

### 3.5. Participants

Participant name	Participant short name	Country	Participant number
THALES Research & Technology	TRT	France	1
Thales Optronics SA	TOSA	France	5
STMicroelectronics Srl	ST	Italy	6
Intracom SA Telecom Solutions	ICOM	Greece	18
Deutsche Thomson OHG	DTO	Germany	20
Alcatel-Lucent Deutschland AG	ALU	Germany	21

PACT XPP Technologies AG	PACT	Germany	7
M2000	M2000	France	8
Associated Compiler Experts bv	ACE	The Netherlands	9
CriticalBlue	CBlue	United Kingdom	10
ARTTIC	ART	France	16

Universität Karlsruhe	UK	Germany	11
Technische Universiteit Delft	TUD	The Netherlands	12
Commissariat à l'Énergie Atomique - LIST	CEA	France	13
Université de Bretagne Occidentale	UBO	France	14
Universita di Bologna	ARCES	Italy	15
Technische Universität Braunschweig	TUBS	Germany	17
Technische Universität Chemnitz	TUC	Germany	19

### 3.6. Project first results

The first annual review took place on 28-29 March 2007, the second annual review of the project was held on 4 March 2008. The most current results of the project, presented during the second review, are the following:

The reference application platforms have been demonstrated, notably the FlexFilm FPGA-based de-noise video platform by Universität Braunschweig and Thomson, the Terapix FPGA-based platform by THALES. These platforms were also presented at DATE conference (10-14 March 2008). The two other application platforms were not shown at the review.

The architecture of the MORPHEUS chip (see figure below) is specified. It notably includes ARM9 controller, 3 various-grain reconfigurable units (M2000 eFPGA, ARCES PICOGA and PACT XPP), software-based dynamic reconfiguration, NoC based interconnect and possibility for Dynamic Frequency Scaling. HDL development now permits to tackle with block level place and route activity and global floorplan. Floorplan of main blocks of the architecture were shown at the review.

The foundry of the chip is planned to be performed through IMAG CMP techno access.

The release 1 of the toolset was also demonstrated, including easy management of dynamic reconfiguration thanks to a tight combination of the Delft University MOLEN implementation on ACE COSY compiler and drivers implemented within the eCOS RTOS by Universität Karlsruhe and THALES. Also, design of configuration of M2000 eFPGA from high level C-based description was demonstrated, based on CriticalBlue CASCADE compiler, THALES SPEAR data mapping tool and MADEO tool by Université de Bretagne Occidentale. Alcatel-Lucent and Universität Chemnitz work on the SpecEdit tool was not shown at the review.

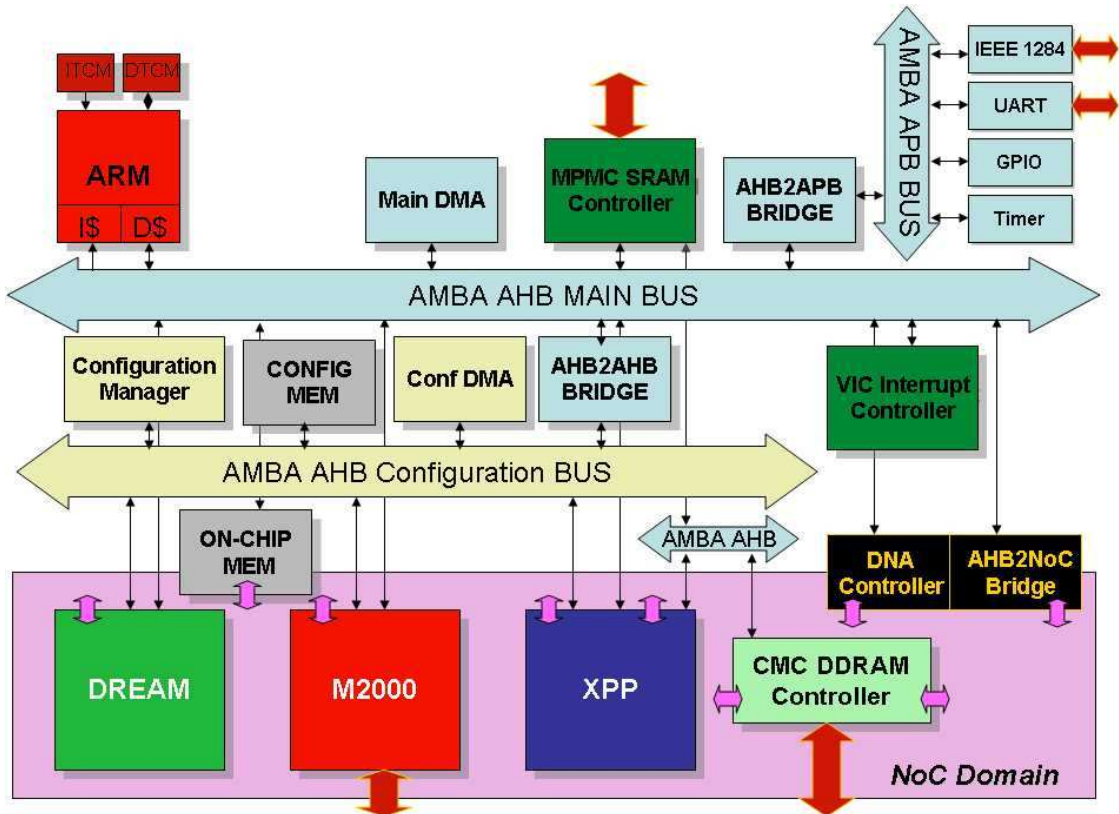


Figure 1 - MORPHEUS chip architecture