MORPHEUS

Abstract of D2.2.1: Computation graph model for high-level Spatial Design input, netlist, circuit, bitstream formats, target environments

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ABSTRACT	This document is the abstract of the D2.2.1. It is available on the MORPHEUS public website
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This deliverable presents the tools developed in task T2.2 “Spatial Design” of WP2 “Tools” of the MORPHEUS project. An overall view on these tools has yet been described in document D2.1.1 “Toolset Specification”.

T2.2 is developing a framework that will

_ move the data from main memory to local accelerator memories

_ move and process data from local memories to local memories across a graph of control and operators (CDFG)

_ and will send back data at the right place in main memory.

The document is organized in four main sections:

_ Spatial Design ambitions

_ tools modules presentation

_ tools interoperability

_ HRE reconfigurable architecture characterization

It will be followed by a description of industrial HRE architectures, based on the tools presented here. This description will be the subject of deliverable D.2.2.2.

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