MORPHEUS

D8.3: Report on MORPHEUS autumn school

CONTRACT NO	MORPHEUS IST 027342
TYPE OF DOCUMENT	Deliverable
DATE	15/04/2008
ABSTRACT	This report summarizes the actions that took place during the MORPHEUS/AETHER autumn school in October 2007.
AUTHOR, COMPANY	Matthias Kühnle, UK
CONTRIBUTORS	Florian Thoma, UK
	Michael Hübner, UK
WORKPACKAGE	WP8
CONFIDENTIALITY LEVEL	PU
FILING CODE	MORPHEUS-UK-D8.3-R1.0.doc
DOCUMENT HISTORY	

Release	Date	Reason of change	Status	Distribution
R1.1	14/01/2008	Creation	On-going	Email
R1.2	10/03/2008	Internal review by ART	Done	Del leader
R1.3	21/03/2008	Reviews accounted	Done	Arttic

Supported by the IST-Programme

Sixth EU Framework Programme for Research and Technological development

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1. Introduction

The First AETHER - MORPHEUS Workshop- Autumn School “From Reconfigurable to Self-Adaptive Computing” (AMWAS'07) was organized in Paris, France in October 8-11, 2007. The innovative "Workshop-Autumn School" format has been chosen to provide participants with both grounding on a new, challenging scientific area and with exposure to research results and proposals. The AMWAS'07 constituted a meeting-point for researchers and graduate students, interested in innovative next-generation computing architectures.

2. Executive summary

This document is a report about the 4 day event, held in Paris, France in October 8-11, 2007 called: AETHER - MORPHEUS Workshop- Autumn School (AMWAS'07). The event has been organized in a two day school as well as a two day workshop. Both events were focused on self-adaptive/dynamically reconfigurable computing architectures. This document gives a summary about the presentations and the speakers. The program committee is listed and attendees' feedback is given.

3. AMWAS 2007

AMWAS 2007 (ÆTHER – MORPHEUS Workshop and Autumn School), “From Reconfigurable to Self-Adaptive Computing” 8-11 October 2007, Paris, France, was a common event organized between the ÆTHER and the MORPHEUS projects. The two projects have many points of common interest: In fact MORPHEUS is focusing on dynamic reconfigurable computing, whereas ÆTHER is studying self adaptive computing systems. Both projects are grounded on computer architecture and software tools. The two projects have in common a set of participants: THALES, CEA-LIST, UK and INTRACOM are in fact participating to both the projects.

The event was organized in two parts: the autumn school on reconfigurable computing and the autumn workshop on reconfigurable computing. The school was more focused on dissemination and training issues with a participation of 33 people, mainly students from the university partners of the two projects. The program of the school included, after the introduction from the coordinators G. Edelin and C. Gamrat, 11 presentations: 5 from MORPHEUS, 5 from ÆTHER and 1 common to both projects. The School was aimed at raising interest among students about a possible involvement in the projects or in possible further developments on reconfigurable computing. Table 1 contains a summary of the contents of the Autumn School; it reports only the parts about MORPHEUS.

3.1. Main goal

Though emphasis was on innovative techniques developed by the AETHER and MORPHEUS research communities, the AMWAS program has not been restricted to the AETHER and MORPHEUS approach but it provided as well a comparative analysis of other proposals and experiences on reconfigurable and self-adaptive computing solutions, from the hardware level to the application level. Researchers and experts working in other EU-funded research projects participated, lecturing on each sub-theme. Various points of view have been presented in after-lecture discussion hours and in focused seminar sessions.

3.2. Main topics

The main theme of the AMWAS'07 deals with the broad subject of "Self-adaptive/dynamically reconfigurable Computing Architectures", focusing more specifically on the problem of self-adaptation at all levels within a system, from hardware architecture to application layer. Knowledge to be provided by the AMWAS refers to "Computing with Adaptive Hardware: Architecture and Software."

The topics were divided into several sub-themes, which were presented from the viewpoint of the various disciplines involved in the main AETHER and MORPHEUS subprojects. The program included the following sub-topics:

- adaptive systems and self-adaptive systems
- static adaptation
- dynamic adaptation
- dynamic reconfiguration and self-adaptivity
- parallelization and allocation of an application onto reconfigurable architectures

3.3. AMWAS autumn school

Self-adaptive, dynamically reconfigurable systems offer the promise of making actually efficient and effective the potential processing power that will be housed on next-generation chips and that risks remaining under-exploited for large segments of applications. By tuning parallelism at run-time to the requirements of the application, one can envision overcoming the low exploitation of resources that often undermines the performances of high-performance chips. At the same time it optimizes such aspects as power consumption, capacity of survival to faults, etc. Yet, to achieve such end, one must set up suitably designed and compiled software, extracting parallelism and providing efficient and robust concurrency management, while simultaneously reconfigurable hardware architectures must be devised to support a self-adaptive, highly parallel mode of operation.

The AETHER-MORPHEUS Summer School provided attendants with insight into innovative software and tools for concurrency management and into architectures for self-adaptivity and reconfiguration, based on research carried out in European projects AETHER and MORPHEUS. Further details on the technical program are given below.

The School targeted in particular PhD students interested in the new and challenging field of self-adaptive and reconfigurable systems. For PhD student who ask to obtain credits from the summer school, assignments have been set up and evaluated.

Presenter – Project	**Title – Contents – Feedback**
K. Bertels TU-Delf	Polymorphic processor and data-parallel mapping
	Presentation about the Molen paradigm.
S. Guyetant, CEA-LIST	Hardware Technologies for Adaptive and Self-Adaptive Computing
	Analysis of adaptability in computing, reconfigurable hardware provides

	advantages in adaptability. You can afford way more complex scheduling algorithms in HW than in SW. Reconfigurable architectures: APTIX, the MORPHEUS platform based on FlexEOS DREAM XPP. Definition of reconfiguration services. Examples: compression, allocation on different resources (PICOGA, FlexEOS, SOFTWARE). Conclusions: reconfigurable architectures provide more programmability and less overload for control and reconfiguration.
D. Picard, UBO	Coarse grain reconfigurable technology Analysis of available architectures (DSP,GPP, ASICS, FPGA, SOC, ASIC-accelerators, ASSP, customizable-processors (Tensilica, ARC) and reconfigurable architecture (DREAM architecture from ARCES). Motivation by comparing the Moore and Shannon law, technology improvement is not enough. DSP is modelled by DFG that can be implemented either in spatial or temporal domain. Special solutions add specialized functional units (Tensilica, ARC). VLIW and superscalar processors provide ILP at compile time or load time, Reconfigurable solutions provide parallelism at run time. DFG can be implementation on FPGA. Reconfigurable architectures introduce the concept of instruction set metamorphosis. Reconfigurable architectures can be fine grained (LUT), coarse grained (data paths) or processor arrays. Examples of reconfigurable architectures. - The GARP architecture - MOLEN approach using Xilinx Virtex-II, a Microcode based application - the Xirisc architecture (ARCES) - RDA reconfigurable data path array (Hartenstein) - piperench architecture (Goldstein) - Pact XPP (Becker Vorbach) array of 16 bit processing elements - Morphosys from UC Irvine - Tilera Tile processor and RAW are array of processors Description of the DREAM small area architecture for crypto and telecommunications applications based on PICOGA (DFG based)
E. Lenormand TRT	SPEAR parallel application mapping tool General presentation about the tool for data streaming applications, it captures the application and the architecture providing an interactive design environment graph of the application. SPEAR helps mapping applications to architecture expressing regular streaming access. Graphs must be acyclic. SPEAR generates the code corresponding to the loops that represents I/O access to data, functions inside the loops are written in C they are mapped to tasks code inside tasks is encapsulated. It is possible to generate again the explicit C code of the SPEAR model. There is a mapping of the loops to processors and data to memories to estimate performances. Insertion of communication, fusion and scheduling, performance simulation obtaining task and data parallelism. The tool computes a static scheduling based on production consumption relationships.
M. Hübner UK	Design Methods and Architectures for Run-Time Adaptive Electronic Systems (Part I and II)
M. Hübner UK	Trends of the ASIC/ASPP market from year 2000. Introduction of the basic terminology about programmable, configurable, reconfigurable and dynamically reconfigurable systems.

Feedback

Proposal of PHD and post-doc available at CEA – LIST and 6 months internship for master students.

Remark for the students that it is worth to focus their studies on reconfigurable computing.

A question was raised if there are advantages of RC in other application fields apart from DSP? The answer was that the actual model is not suitable for control applications.

A question was asked about comparing the proposed solution with the best reference FPGA solutions. Saying that the proposed solutions can be equivalent to new more enhanced FPGA solutions. The answer was telling that MORPHEUS wants to have an implementation to silicon and also to innovate, so it has to choose a starting reference point with FPGA technology at the time of the project start and trying to innovate and implement from that starting point.

This presentation was excellent, but the purpose is not only to collect all the info in one place but to start discussions. Basic problems are the same for many projects. This should be outlined to extract useful experience for other projects also.

It was noticed that there is good complementarities between MORPHEUS and ÆTHER.

For RC it should be useful to forget the legacy part and to focus on new solutions.

A question about SPEAR was asking if it is possible to rearrange the input according to consumption policy. This is not possible currently.

Table 3-1 Content of the Autumn School on Reconfigurable Computing

3.4. AMWAS workshop

The workshop was highly interactive and engaged participants in fruitful discussions on its topics. There was no registration fee for participants. It featured keynote presentations as well as solicited papers, each of them to be presented by one of its authors. The duration of the presentation of each paper has been 20 minutes plus 10 minutes for discussions. Authors submitted an extended abstract of their presentation of about 1000 words to the Workshop Coordinator. Keynote speakers of international renown, not belonging to the AETHER or MORPHEUS community (experts on the field) gave influential talks about their work and/or vision. As closing session of the first day of the workshop, a round table session with the topic "*Future ICT Systems: From Tera ops to Tera processor on chip. What are the main challenges?*" was held. The panel of C. Gamrat, G. Edelin, P. Van Hove, S. Singh and K. Bertels engaged in a lively discussion with the audience on the long-term future of reconfigurable computing.

The School was more focused on training issues and addressing students, the Workshop instead addressed the industrial partners of the two projects, extending the participation to partners of other European projects and to European Commission. Table 2 contains a summary of the contents of the workshop; it reports only the parts about MORPHEUS.

A. Grasset THALES	**A Framework for Memory Based Mapping of Accelerated Function** Nested loops often compose the computation intensive part of digital signal processing applications. Accelerating these loops kernels on specific hardware coprocessors bring gains in performances but lacks flexibility. Reconfigurable units provide a new trade-off in term of performances, cost and flexibility in System-on-Chip. However, programming these heterogeneous reconfigurable units is time consuming and error prone. Managing memory mapping and the addressing mechanism of multidimensional arrays is an issue on these kinds of systems due to their strong constraints on memory. In this context, high-level synthesis of functions on reconfigurable accelerators is interesting to reduce the time for application development. A design flow is developed in the MORPHEUS project in parallel to the MORPHEUS reconfigurable architecture. This flow covers the CPU programming and the high-level synthesis of the accelerated functions on reconfigurable units. The synthesis flow of the accelerated functions separates computation and communication issues, In the MORPHEUS platform, local buffers attached to three

heterogeneous reconfigurable units are used for the communication. The talk describes a framework integrated in this flow which helps to manage communications and memory mapping related to the implementation of the accelerated functions on the reconfigurable units.

D. Picard

UBO

Process Networks on a Reconfigurable SoC

The execution of an application on a reconfigurable SoC can be modelled as a set of coordinated processes. Some of these processes effectively run on the reconfigurable units, others are idle waiting for input data or synchronization conditions, while the remaining are suspended, and perhaps do not have hardware resources allocated. Processes need communication and synchronization mechanism to coordinate, but in some cases these mechanisms can be simple. It is the case if the application has been defined as a stream of structured data flowing into a pipeline of processes due to memory modes. In other cases, the system can be much more complex with typical synchronization problems appearing either at the application level and the system support level. The reconfigurability of the hardware even gives more importance to this question because race conditions can appear between the OS and the application behaviours. Thus, it is needed to develop a system methodology inside and outside the tool. This paper describes a pragmatic approach where the spatial process organization is specified separately from their behaviours. The organization allows naming processes and binding them to a behaviour. The connectivity between processes defines the knowledge established in the system, and as a matter of facts, the communication links used to propagate this knowledge. This part of the system description is fixed in a model and grammar called AVEL. The talk presented the MORPHEUS architecture based on Dream-XPP-M2000, introducing the control data flow generator and presenting the generation of the CDFG from AVEL through the SyNE tool.

U. Pross

TU Chemnitz

Prototype of a Dynamically Reconfigurable Network Node

Current high-end telecommunication networks like other digital technologies tools are subject to a rapid evolution. The requirements for these networks increase permanently in terms of transfer rate, security and quality. This evolution requires the development of new network standards or the adaptation of existing standards. On one hand, standardization processes take a long time. Manufacturer of telecommunication equipment, who want early market presence, are often not able to wait until the end of the standardization process. Instead they have to implement standards which are not stable and might be adapted or changed in future. This causes a high business risk since a later adaptation of the standard may require a new implementation. However, the later the standard change occurs in the development cycle, the more expensive a reimplementation and its new production are. On the other hand, reimplementation can be caused by implementation mistakes as well. The risk of a reimplementation can be drastically reduced by the usage of reconfigurable technologies in integrated circuits. This presentation was about the implementation of a node which can be dynamically configured using the Ethernet protocol.

M. Kühnle

University Karlsruhe

A System on Chip Decoder – a project oriented SoC design for education

A good hardware design requires both competent theoretical as well as practical knowledge in the areas of architecture specification and design. While the theoretical background is given in many lectures, gaining practical knowledge is somewhat more difficult. Also connection points to research can be given more easily in such practical work by building a bridge to the latest research projects such as MORPHEUS, etc, where many similar development tasks exist. Also the application driven design is well covered by an audio system and can be well compared, although much less complex – to e.g. multimedia applications within MORPHEUS. Facing these facts, a laboratory has been established. Hardware and Software components have to be realized to build up a SoC for audio decoding. The goal of this laboratory is to make students familiar not only with practical aspects of HW/SW ASIC design flow. So, insight is given into different design methodologies and technologies starting from design space exploration through IP block integration to system verification. Also different design flows (FPGA based, standard cell based) are introduced. As used in MORPHEUS, the students are made familiar with the same state of the art development tools. Summarizing, the realization of the system provides a good base to study HW/SW Co-Design techniques in hands-on fashion. Although the content of the laboratory deals with complex topics (very close to project work), which require a good preparation and concentrated work of the students, the feedback was throughout very positive.

Feedback

Some questions were asked about the course organization and the attendance.

How are students curricula affected?

The training is embedded in FPGA standard courses, courses for HW/SW co-design and courses for integration with the MORPHEUS project are affected. The feedback from the students is positive because they have access to a huge/complete design experience with adequate documentation. Every student has one board available and there is one trainer every five students. The course lasts three weeks.

A remark was added saying that it would be interesting to use the MORPHEUS platform in the courses. We don't have this possibility right now but it be possible when we have the simulator.

How did you manage the project organization? Through three steps: specification-documentation-implementation.

G. Pulini

M2000

The M2000 FPGA – A New Direction in FPGA Architectures

Almost all FPGA architectures use LUTs (lookup tables) to implement logic circuit functionality. What differentiates them is their interconnect architecture, and it has been apparent for many years that the cost, performance and power of deep submicron FPGAs are dominated by their interconnect architecture. M2000 has redefined FPGA interconnect architectures using a recursive, hierarchical interconnection scheme that scales much better than the grid-based interconnect architecture of traditional FPGAs. This produces much better logic density, resulting in better performance and lower power. This talk describes this novel interconnect architecture, and how it is used to provide flexible, high bandwidth connections between logic elements in large-scale FPGAs. We also discuss the functional components provided by the M2000 architecture, which include fast addition and multiplication as well as embedded dual port memories. Finally, the support for dynamic reconfiguration is discussed along with example applications.

Feedback

G.Pulini M2000 answers to questions:

Do you have a plan for developing coarse grain also? Not for the moment.

What about the density? We create a product that is different from current solutions in the market; it is denser having 800K LUT in a device.

Do you add partial reconfiguration also? This is a recurrent question. We are looking into it.

L. Lagadec

UBO

Portable Synthesis in MORPHEUS

MORPHEUS promotes the transparent use of heterogeneous reconfigurable resources in system on chip. Given the variety of reconfigurable architectures and low level specification languages, it is necessary to use a robust methodology to isolate the application description languages from the possible targets. The WP2 consortium has adopted the idea of a common format for algorithm description that could be used as a cross-point for sources and targets. This format is a kind of Control Data Flow Graph address by an application programming interface. An input language compiler can then generate processing description to this API producing library or files for the synthesis tools. As for now several tools output CDFG description: Cascade from CriticalBlue, SPEAR from Thales TRT, SpecEdit from Alcatel Lucent, AVEL (concurrent process system description environment). This talk presents the WP2 flow from the CDFG down to the synthesis over IPs and especially over MP2000 IP. This goes through defining the CDFG structure (formal description in EXPRESS) and its associated tools (rules checker, interchange via STEP files). Also transformations performed over specific CDFGs are introduced: partitioning, mapping ordering, scheduling and synthesis.

M. Hübner

University Karlsrühe

On-line Routing of Reconfigurable Functions for Future Self-Adaptive Systems

The progress in hardware technologies for implementing portable, low power and low cost electronic systems for consumer products has been major the last years. The complexity of embedded systems further increase at a rate which is not met by the development of advanced CAD tools for managing the large design space. This likely lead to increased design problems regarding system implementation, test and verification. This talk presents how the design complexity can be managed at the hardware level by integrating self-adaptive characteristics, and how the trade-off in performance and flexibility can be optimized to fulfil all application requirements while reducing the design complexity.

E. Schüler

PACT

XPP-III Basics and SoC Integration

Application and market requirements are driving the deployment of the new architectures when existing solutions cannot fulfil the actual needs. “Reconfigurable Computing” is one answer to the ever increasing application requirements. In addition to the well understood FPGAs, also coarse grain architectures are now ready to be adopted into the computing mainstream. During this session, we present the third generation of XPP, one of the first coarse grain reconfigurable architectures. XPP-III is built from an array of ALUs and RAMs with a programmable interconnect. The array is configured statically and data to be processes streams through the network of operators. The programming model is based on direct mapping of data flow graphs to the array. Larger algorithms are partitioned into several graphs which are dynamically reconfigured. This way of processing provides a very high degree of parallelism for algorithms such as FFTs, filter, raw pixel processing etc. In addition to the reconfigurable array new VLIW-similar processing elements are tightly coupled to the array. Those processing elements provide parallelism for algorithms which are sequential by nature and where a large number of decisions must be made. Examples are parsers, protocol handling, arithmetic decoders etc. The combination of both types of processing elements extends the application space of the reconfigurable array substantially. Even as important as the raw processing power is the integration into SoC and the memory hierarchy. We present a framework of building blocks and a network for streaming data that allows flexible integration into any SoC and memory architecture. Two examples are shown, the integration in the MORPHEUS SoC and the XPP-3C accelerator chip. The programming concept and the native tools and APIs to program this versatile architecture are shown. The complete XPP-III platform be available in a SystemC based software simulator which allows not only standalone simulation of the XPP but also the integration into a SoC simulation environment which be demonstrated in the MORPHEUS project.

Feedback

A few questions have been asked.

Besides this involvement in MORPHEUS, do you deliver an IP or a chip? PACT delivers both of them.

Which is the time schedule for the MORPHEUS IP? The chip will be available next year.

S. Witty

TU Braunschweig

High Speed DDR-SDRAM Memory Controller for the MORPHEUS Platform

Applications designed for the MORPHEUS platform may require a massive amount of memory, as well as sufficient bandwidth, to fully demonstrate MORPHEUS' potential as a high performance reconfigurable architecture. For example, the film grain noise reduction application, which is composed of multiple image processing tasks, requires massive amounts of bandwidth due to its real time requirements. To meet these requirements and to eliminate external memory bottlenecks, a high bandwidth DDR SDRAM memory controller (CMC) has been designed for use in the MORPHEUS platform.

C. Teodorov

UBO

Quick Integration of High Level Tools in MORPHEUS: The case of SpecEdit

MORPHEUS promotes the transparent use of heterogeneous reconfigurable resources in SoC. Given the variety of reconfigurable architectures and low level specification languages, it is necessary to use a robust methodology to isolate the application description languages from the possible targets. The WP2 consortium has adopted the idea of a common format for algorithm description that could be used as a cross-point for sources and targets. This format is a kind of Control Data Flow Graph (CDFG) addressed by an application programming interface (API). An input language compiler can then generate processing description to this API producing library of files for the synthesis tools. The aim of this paper is to demonstrate the method we follow to integrate new environments to MORPHEUS.

	The tool SpecEdit is build around a formalism called ADeVA (Advanced Design and Verification of Abstract Systems) from Alcatel Lucent. Its aim is to allow specifying and verifying complex state machines from simple composition of processes interacting with the environment. This formalism has been represented as a set of Smalltalk 80 classes that have been derived from an XML output of SpecEdit. As a practical result, it is now possible to generate CDFG representing the SpecEdit specification. The example of a traffic light controller is used to illustrate this transformation.
L. Lagadec	**Mapping to a Reconfigurable IP**
UBO	Integrating external components in a system on chip is a challenge at both the chip level and the software tool chain. In the MORPHEUS project, a generalized approach has been developed using CDFG as a computation representation and tools dedicated to the mapping of computations to components. In this paper, we describe two different techniques used to integrate respectively the PiCoGA array and the XPP-IIb datapath in the tool chain. Each technique based itself on the component programming interface and documentation, giving varying degrees of knowledge and control over it, and, importantly, being more or less difficult to implement. The results demonstrate the feasibility of the concept of a unified tool chain. Such results allow SoC designers to evaluate how effective and complex the integration of a component into the tool chain is, and, for the developer of a component proposed for integration, which level of documentation or access to the component it the most competitive for a prospective SoC designer makes.

Table 3-2 Content of the ÆTHER MORPHEUS Workshop

3.5. Program Committee

Michel AUGUIN (Centre National de la Recherche Scientifique - CNRS)

Jürgen BECKER (Universität Karlsruhe - TH ITIV)

Koen BERTELS (TU Delft)

Joan CABESTANY (Universitat Politècnica de Catalunya - UPC)

Gilbert EDELIN (THALES Research & Technologies - TRT)

Rolf ERNST (TU Braunschweig)

Christian GAMRAT (Commissariat à l'Energie Atomique - CEA LIST)

Roberto GUERRIERI (University of Bologna)

Ulrich HEINKEL (TU Chemnitz)

Chris JESSHOPE (Universiteit van Amsterdam - UvA)

Jiří KADLEC (Akademie věd Česke Republiky - ÜTİA AV CR)

Bernard POTTIER (university Bretagne, O.)

Mariagiovanna SAMI (Università della Svizzera italiana - USI)

Alex SHAFARENKO (University of Hertfordshire - UH)

Patrick VAN HOVE (EU Commission)

4. Concluding section

4.1. Conclusion

This event has been a great success and it was well appreciated by the auditorium. Consequently, a next workshop and school is planned in summer 2008.

4.2. Glossary

ACA	Advanced Computer Architectures
ADeVA	Advanced Design and Verification of Abstract Systems, a state/transition based language for system specification from ALCATEL-LUCENT
AES	Advanced Encryption Standard
ÆTHER	Self-Adaptive Embedded Technology for Pervasive Computing Architectures
AHB	Advanced High-performance Bus
AMBA	Advanced Microcontroller Bus Architecture
AMWAS	ÆTHER MORPHEUS Workshop and Autumn School
ANSI	American National Standards Institute
API	Application Programming Interface
APTIX	An FPGA platform
ARC	Configurable processor
ARCES	Advanced Research Center on Electronic Systems
ARCS	Architecture of Computing Systems conference
ARM9	Processor family
ASICs	Application Specific Integrated Circuits
ASSP	Application Specific Signal Processor
Atmel	Semiconductor industry
AVEL	Concurrent process system description environnent
C	A computer programming language
CAD	Computer Aided Design
CASCADE	Embedded software design tool by CBlue
CASTNESS	Computing Architectures and Sw Tools for Numerical Embedded Scalable Systems: a dissemination event promoted by SHAPES EC project
CDFG	Control Data Flow Graph
CMOS	Coupled Metal Oxide Semiconductor
CONQUEST	International conference on Quality Engineering in Software Technology
ConvergenSC	Design tool
CoWare	Design tool
CPU	Central Processing Unit
CRC	Cyclic Redundancy Check
CS	Computer Science

DATE	Design Automation and Test Europe: it is the most important conference in Europe about design automation
DFG	Data Flow Graph
DoW	Document of Work: it is the fundamental document that establishes the organization, workflow and expected achievements in the MORPHEUS project
DDR	Double Data Rate
DMA	Direct Memory Access
DRAM	Dynamic Random Access Memory
DREAM	The next version of PiCoGA for DSP
DRS	Workshop on Dynamically Reconfigurable Systems
DSP	Digital Signal Processing
DWT	Discrete Wavelet Transformation
EB	Executive Board: a committee composed of the coordinator and work package leader within the MORPHEUS project
EC	European Community
eCos	a real time operating system
EDA	Electronic Design Automation
ECSI	European Electronic Chip & Systems Initiative
eFPGA	Embedded FPGA
ERSA	International Conference on Engineering of Reconfigurable Systems and Algorithms
Ethernet	Distributed packet-switching protocol for local computer networks
EURASIP	Journal of Embedded Systems
EXPRESS	Language to express CDFG
feast	Forum for European-Australian Science and Technology cooperation
FEC	Forward Error Correction
FET	Future and Emerging Technologies
FFT	Fast Fourier Transform
FlexEOS	embedded FPGA macro from M2000
FlexFilm	TUBS project addressing the development of systems for flexible real-time processing of digital film at high resolution
FP	Framework Program
FPGAs	Field Programmable Gate Array
fps	Frames per second
FPL	Field Programmable Logic and applications conference
Gbit/s	Giga bit per second
Gops/s	Giga operations per second
GPPs	General Purpose Processors
Griffy-C	C-like data flow language

HDL	Hardware Description Language
HoneyComb	Reconfigurable cellular architecture
HW	Hardware
IEEE	Institute of Electrical and Electronic Engineers
ILP	Instructin Level Parallelism
IP	Intellectual Property: it defines any formalized reusable knowledge (hardware, software, or process)
IP	Internet Protocol
IO	Input Output
IRISA	Institut de recherche en informatique et systèmes aléatoires
ISA	Instruction Set Architecture
IST	Information Society Technologies: a priority within the framework program of European research activities
LUT	Look Up Table
MADEO	Specification architecture tool from UBO
MOLEN	Reconfigurable processor paradigm developed at TU Delf
MORPHEUS	Multi-purpose dynamically Reconfigurable Platform for Intensive Heterogeneous Processing
MOTES	Workshop on Model based Testing for Systems.
MPEG	Motion Picture Expert Group
MPSOC	Multi Processors System on Chip: an international forum about multi-processor applications for system on chip
NASA	National Aeronautics and Space Administration
NoC	Network on Chip
NP	Network Processor
NRE	Non Recurrent Engineering (costs)
NuSMV	Symbolic model checker
OS	Operating System
PAR	Periodic Activity Report
PE	Processing Element
PO	Public Officer
QoS	Quality of Service
QUKU	Coarse Grained PE array overlaid on FPGA fabric
RC	Re-configurable Computing
RCEducation	Conference on Reconfigurable Computing Education
Rijndael	Block cipher algorithm used in AES
RISC	Reduced Instruction Set Computer
RTOS	Real Time Operating System
PCI	Peripheral Component Interconnect

PiCoGA	Pico Gate Array: reconfigurable processing element by ST
QSIC	Quality Software International Conference
SAMOS	Embedded Computer Systems: Architectures, Modeling and Simulation: conference on embedded systems, hardwre/software co-design, compilation, embedded reconfigurable processors, modelling languages …
SANE	Self-Adaptive Network Entities
SBCCI	Symposium about integrated circuits and systems design
SDRAM	Synchronous Dynamic Random Access Memory
SEB	Steering and Exploitation Board a structure, appointed from the GA, to ensure that the objectives of the MORPHEUS project are fulfilled.
SEW	Software Engineering Workshop
SHAPES	Scalable Software Hardware Architecture Platform for Embedded Systems: a FET-ACA IST-FP6 Integrated Project started in January 2006
Smalltalk	A programming language
SoC	System on Chip
SPEAR	TRT tool mapping an application on a parallel programmable processing architecture
SpecEdit	Design specification tool
SRAM	Static Random Access Memory
SQS	Software & System Quality Conference
STEP	Intermediate format expressing CFDG for MADEO
SyNE	Tool that generates CDFG from AVEL
SystemC	System modeling language
SW	Software
Tensilica	Configurable processor
TRT	Thales Research & Technology
UNICAD	UNIfied Computed Aided Design: workshop organized internally to ST
Virtex-II	Xilinx FPGA platform
Virtex-II Pro	Xilinx FPGA platform incorporating PowerPC processor
VLIW	Very Long Instruction Word
WiMAX	Worldwide Interoperability foe Microwave Access
WP	Work Package
WPPA	Weakly Programmable Processor Array
WWW	World Wide Web: the internet network
Xilinx	Company providing FPGAs
XiRISC	VLIW reconfigurable processor architecture by ST
XPP	eXtreme Processing Platform

Table 4-1 Glossary