



# MORPHEUS

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## D5.5.3: Phase 2 specification of application test case subsets

### 8. Appendix 1: PUBLISHABLE ABSTRACT

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### Context

This deliverable is part of the MORPHEUS project which is a european initiative financed under the 6th FP and addresses innovative solutions for embedded computing based on dynamically reconfigurable platform and tools.

MORPHEUS project aims at satisfying embedded systems new demanding requirements in terms of computing performance, cost-efficient development, functional flexibility and sustainability by developing a global solution based on a modular heterogeneous SOC platform providing dynamically reconfigurable computing completed by a software oriented design flow and a consistent toolset.

MORPHEUS is a 3-year project started in 2006 and gathering all the required expertises from several countries : academics, industrials, SMEs.

## Aim of the deliverable

The goal of this document is to provide details concerning the specification of the four case studies that will be used as testing vehicle for the final MORPHEUS platform and the associated toolset. Based on the experience gained from the implementation on COTS platforms during phase 1, the end users of the MORPHEUS consortium have selected appropriate subsets of their application in order to take advantage of the MORPHEUS state of the art technology.

## Content of the deliverable

For ICOM's case study, the functionality targeted in phase 2 of the MORPHEUS project focuses on a part of the physical layer of IEEE 802.16j standard. Specifically the blocks that handle continuous streams of complex time-domain data in the Mobile Station receiver chain front-end will be simulated by ICOM on the MORPHEUS platform. The type of processing implemented includes a word-level processing block (FFT) and bit-level processing blocks (e.g. derandomizer).

After a short summarization of phase 1 the network routing application dealing with the broadcasting of configuration data via network infrastructure by ALU/TUC is described focussing on phase 2. The specification is described in a first approach. Further details will be worked out in the upcoming months. Challenges like the limited area of the 4K embedded FPGA macro are addressed. While most parts of the phase 1 demonstrator have already been synthesized for the macro, some parts being specifically needed in phase 2 are still under development.

In phase 2, TOSA intends to simulate the MORPHEUS phase 1 motion detection test case application on the MORPHEUS chip simulator using the MORPHEUS toolset, and to take detailed measurements in order to assess the performance of the final MORPHEUS chip against the COTS based implementation. The selected subset of phase1 test case is composed of the whole motion detection algorithm adapted to the processing of two images instead of video processing. This small adjustment allows being very close to the phase1 implementation and allows comparisons with phase1 implementation.

The professional film/video application provided by DTO and TUBS for the 2<sup>nd</sup> phase of the project is described, motivated, and characterized. The selected application implements typical algorithms for video and picture processing as Motion Estimation / Compensation and Direct Wavelet Transformation. For this reason this application was chosen as one of the two MORPHEUS applications that finally will be mapped onto the MORPHEUS silicon platform. Further, based on the experiences of the 1<sup>st</sup> project phase some performance and reconfiguration requirements are specified for the implementation on the MORPHEUS chip.