
# MORPHEUS

## Abstract of D5.3: Report on selected implementation platforms and application subsets partitioning

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| ABSTRACT | This document is the abstract of the D5.3. It is available on the MORPHEUS public website |
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Deliverable 5.3 describes the intermediate platforms of each application partner. These platforms are based on components of the shelf (COTS) as microprocessors, FPGAs, memories etc, and are intended to be a state-of-the-art benchmark and reference for the MORPHEUS platform.
These platforms are intended to evaluate certain, selected concepts at an early stage of the MORPHEUS project with using the metrics defined in D5.2. Furthermore it allows a bottleneck analysis, which goes beyond mere simulation-based approaches.
All the contributions are structured into subsections dealing with the following topics:

- A detailed description of the intermediate platform, to give a first detailed overview of the platforms' capabilities. Thereby, the presented platforms are mainly FPGA-based.
- An analysis of how to partition the application with respect to reconfiguration, which focuses on the concepts that are especially suited for reconfiguration or take advantage of the reconfiguration.
- The intended partitioning for the concrete implementation of the application on the selected intermediate platform.
- A link between the intermediate platforms of phase 1 towards the MORPHEUS platform of phase 2.

For the three applications it is planned that each of the reconfigurable IP cores, which comprise the M2000 embedded FPGA, the PiCoGA and the PACT XPP, is at least used in more than one application. In addition all applications make use of the ARM 9 embedded RISC processor, the memory subsystem and the Network-on-Chip (NoC), which are introduced in deliverable D3.1. Therefore, a good coverage among the different test cases is guaranteed to allow giving more profound statements about the benefit and usability of the MORPHEUS platform.

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