



# MORPHEUS

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## Abstract of D3.4: Architectural Metrics for Interconnect

CONTRACT NO	MORPHEUS IST 027342
TYPE OF DOCUMENT	Publishable abstract of D3.4
DATE	08/06/2007
ABSTRACT	This document is the abstract of the D3.4 It is available on the MORPHEUS public website
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WORKPACKAGE	WP3
CONFIDENTIALITY LEVEL	RE
FILING CODE	MORPHEUS-D3.4-UK-R2.1



The deliverable's results are complexity estimations and performance – area dependency declarations for the network as used in the platform. In the beginning, some challenges are identified. Further application and computation engine requirements are recalled carried on and clearer specified. Thereto deliverable 5.2 has been analysed and used as basic input. Considering this document, it becomes clear that requirement vary a lot depending on the application. Also it hasn't been trivial to extract bandwidth demands from the given requirements. Lucent for instance will use mainly the eFPGA for implementing their algorithms. So, from their side communication links need to be guaranteed between eFPGA and on-chip/off-chip memory, whereas Thomson has complementary requests using rather the PACT XPP for their streaming approach. So, a trade-off has been found, that satisfies all requirements adequately. This resulted in a ten node network with an intelligent alignment of the different IPs.

Also, the simulation environment as used for NoC simulation is quickly explained from where the features of the NoC and its components could be deeply investigated. This allowed complexity estimations and resulted in the upper described topology and configuration proposal. Hereby, adaptations related to the original implementations are outlined and possible topologies are shown. The fully configured 24 node network as proposed in deliverable 3.2 has been further examined and finally considered not only to complex in terms of area but also oversized in terms of the provided performance compared to the requirements. After all, simulation results helped to enable the network IP dimensioning and showed dependencies between area occupation and performance, hence the efficiency of the NoC. Explicitly, the NoC can be configured in an area saving way, since no congestion can take place in the MORPHEUS SoC. Moreover, the channel bandwidth of around one Gbyte/s per channel has been the basis for a mostly one-to-one mapping solution, which means that generally one NI is sufficient per IP that is connected to it. The PACT XPP, the external memory controller will use two network connections. Also two connections are foreseen for on-chip ram. As already mentioned above, this results in a 10 node STNoC, where two possible configurations have been found through simulation. The basis configuration occupies 18k gates per router and 14k gates per NI. The second configuration occupies 10% more area and increases the throughput performance of around 6%. So, a summarized recommendation is the following: If area occupation doesn't play a major role within the quoted range (the difference between the 2 proposed NI and router compositions), the 2nd STNoC configuration for all NoC components can be chosen. This will help to improve the performance for a few traffic patterns. On the other hand, the performance outcome of the basic configuration will be able to meet the requirements of the applications that are described in the outlook on the usage of the MORPHEUS platform within deliverable 5.3. However an extended use of the interconnect may be beneficial and desired by modified applications in future and therefore – if not constrained by the budget – the more sophisticated and slightly more area demanding STNoC configuration should be focused on.

