



# MORPHEUS

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## **Abstract of D4.1: Status of MORPHEUS development and State of the Art**

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ABSTRACT	This document is the abstract of the D4.1. It is available on the MORPHEUS public website
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The MORPHEUS platform is a complex System-on-Chip that exploits run-time programmability at different levels to provide a competitive computing solution, that can challenge developments costs of application specific silicon platforms through product customisation after fabrication.

MORPHEUS ambition is to deliver computational power competitive with state-of-the-art programmable Systems-on-Chip maintaining flexibility to a broad spectrum of applications, and user-friendliness.

For this reason, the main references for the evaluation of MORPHEUS will be:

- a) Commercial FPGA-based processing platforms such as Xilinx Virtex and Altera Stratix.
- b) DSP oriented programmable systems-on-chip such as OMAP by TI, Nomadik (STn88xx) or GreenSide (STW21000) by ST, PXA by Intel, the Cell processor by IBM..
- c) Interconnect-oriented multicore platforms, such as RAW by MIT, Imagine by Stanford University, PicoChip, Pleiades by UCB.

The backbone of the MORPHEUS platform is composed by a processor-based architecture built around an ARM core, controlling a set of 3 heterogeneous run-time programmable computation engines linked by high speed interconnect. This backbone is completed by a set of hardware (memory hierarchy, interconnect strategy, dynamic configuration management) and software (compiler, RTOS, configuration toolset) services to enable full exploitation of computation resources without compromising user-programmability.

The programming model of the platform is organized at two levels, according to the Molen programming paradigm that was chosen as reference for application deployment: Macro-code and Micro-code. **Macro-kernels** are high level application programs described in C and run on the ARM processor. *Elementary operators* at this level are computations that are run on the reconfigurable units or data transfer instruction run on the interconnect resources. *Elementary operands* are sets of data, organized in *Streams* or *Chunks*, computed on the reconfigurable units and transferred through the interconnect architecture and memory subsystem. The high diffusion of ARM-based platform in the embedded world makes this approach friendly to the average DSP algorithm developer. **Micro-kernels** are, according to the Molen terminology, micro-coded operations, that are specific application kernels mapped on the specific HREs and then utilized as library components when programming at macro-code level. In this way, it is possible to hide to the end-user heterogeneity in the definition of hardware specific libraries, while retaining hardware specificity at low level to map appropriately each application, or better, each given kernel belonging to a given application.

For these reasons, the monitoring of the MORPHEUS development and comparative analysis with respect of the state of the art has been performed at different levels:

On one side, MORPHEUS relies on a state-of-the-art reference infrastructure consisting in the ARM processor environment, its peripherals, RTOS and standard application development tools



(compiler, debugger, performance evaluation). This aspect will be evaluated in this deliverable in terms of efficiency, usability and diffusion in the SoC market: in this context no innovation is required, but rather strict compliancy to what requested to top-class processing platforms and a low risk margin in technology deployment.

On the other hand, the three hardware programmable computational engines are imported in the project as IPs. Their selection is a specification for the project, although their internal features provide a significant added value with respect to reference competitors. Thus, they will be briefly evaluated with respect to alternative computing solutions.

Finally, the aspect of the platform where the most significant innovation resides, is the exploitation of the heterogeneous computational engines in the context of an integrated homogeneous system. This aspect, that strongly involves both architectural and toolset issues provides the larger added value to MORPHEUS. For this reason, their design must allow the higher margin of risk to provide innovative concept that can lead to better commercial exploitation of the final result. Consequently, the central sections of this deliverable are strongly focused on the assessment of these efforts with respect to the latest related offers both in industry and academia.

